Claims

What is claimed is:

[c1] An apparatus for modeling a power system of a microprocessor based system, comprising:

a plurality of power converter models;

a board model that receives an output from the plurality of power converter models;

a package model that receives an output from the board model; and

a chip model that receives an output from the package model.

[c2] The apparatus of claim 1, wherein the plurality of power converter models comprises a plurality of DC to DC power converter models.

[c3] The apparatus of claim 1, wherein the plurality of power converter models comprises four DC to DC power converter models.

[c4] The apparatus of claim 1, wherein the chip model further comprises:

a plurality of bump and grid models;

a plurality of section models that receives a plurality of outputs from the plurality of bump and grid models; and

a plurality of channel models that interconnect the plurality of section models.

[c5] The apparatus of claim 4, wherein the plurality of bump and grid models comprises nine bump and grid models.

[c6] The apparatus of claim 4, wherein each of the plurality of section models further comprises a load model.

[c7] The apparatus of claim 6, wherein the load model comprises a voltage controlled resistor.

[c8] The apparatus of claim 6, wherein the load model comprises a current source.

[c9] The apparatus of claim 4, wherein the plurality of section models are arranged in an interconnecting grid.

[c10] The apparatus of claim 9, wherein the interconnecting grid is generally square shaped.

[c11] The apparatus of claim 4, wherein the plurality of section models comprises nine section models.

[c12] The apparatus of claim 11, wherein the plurality of the section models are arranged in a three section by three section grid.

[c13] The apparatus of claim 4, wherein the plurality of the channel models comprises ten section models.

[c14] An apparatus for modeling a power system of a microprocessor based system, comprising:

means for modeling a power converter;

means for modeling a board that receives an output from the means for modeling a power converter;

means for modeling a package that receives an output from the means for modeling a board; and

means for modeling a chip that receives an output from the means for modeling a package.

[c15] A method for modeling a power system of a microprocessor based system, comprising:

modeling a plurality of power converters;

modeling a board that receives an output from the plurality of power converter;

modeling a package that receives an output from the board; and

modeling a chip that receives an output from the package.

[c16] The method of claim 15, wherein the plurality of power converters comprises four DC to DC power converters.

[c17] The method of claim 15, wherein modeling a chip that receives an output from the package further comprises:

modeling a plurality of bump and grid components;

modeling a plurality of chip sections that receives an output from the plurality of bump and grid components; and

modeling a plurality chip channels that interconnects the plurality of chip sections.

[c18] The method of claim 17, wherein modeling a plurality of chip sections forms a generally square shaped grid.

[c19] The method of claim 18, wherein the generally square shaped grid comprises a three section by three section grid.

[c20] The method of claim 17, wherein modeling a plurality of chip sections further comprises modeling a load.

[c21] The method of claim 20, wherein the load is modeled as a voltage controlled resistor.

[c22] The method of claim 20, wherein the load is modeled as a current source.

[c23] An apparatus for modeling a power system of a microprocessor chip, comprising:

a plurality of bump and grid models;

a plurality of section models that receives a plurality of outputs from the plurality of bump and grid models; and

a plurality of channel models that interconnect the plurality of section models.

[c24] The apparatus of claim 23, wherein the plurality of section models further comprises a load model.

[c25] The apparatus of claim 24, wherein the load model further comprises a voltage controlled resistor.

[c26] The apparatus of claim 24, wherein the load model further comprises a current source.

[c27] The apparatus of claim 23, wherein the plurality of section models are arranged in an interconnecting grid.

[c28] The apparatus of claim 27, wherein the interconnecting grid in generally square shaped.

[c29] The apparatus of claim 23, wherein the plurality of section models comprises nine section models.

[c30] The apparatus of claim 29, wherein the plurality of section models are arranged in a three section by three section grid.

[c31] An apparatus for modeling a power system of a microprocessor chip, comprising:

means for modeling a plurality of bumps and grids;

means for modeling a plurality of sections that receives a plurality of outputs from the plurality of bumps and grids; and

means for modeling a plurality of channels that interconnect the plurality of sections.

[c32] A method for modeling a power system of a microprocessor chip, comprising:

modeling a plurality of bump and grid components;

modeling a plurality of chip sections that receives an output from the plurality of bump and grid components; and

modeling a plurality chip channels that interconnect the plurality of chip sections.

[c33] The method of claim 32, wherein modeling a plurality of chip sections forms a generally square shaped grid.

[c34] The method of claim 33, wherein the generally square shaped grid is a three section by three section grid.

[c35] The method of claim 32, wherein modeling a plurality of chip sections further comprises modeling a load.

[c36] The method of claim 35, wherein the load is modeled as a voltage controlled resistor.

[c37] The method of claim 35, wherein the load is modeled as a current source.